IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Masahiro Ishida, et al.
Serial No.:	09/699,077
Filing Date:	October 27, 2000
Title:	Method and Apparatus for Fault Simulation of Semiconductor Integrated Circuit
Conf. No.	9031

Examiner: Ayal I. Sharon

Art Unit: 2123

March 24, 2005
San Francisco, California

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR EXTENSION OF TIME

Applicants request a two-month extension of time in which to submit this Response to Office Action. This extension extends the deadline for submission until April 3, 2005. You are authorized to charge the extension-of-time fee to deposit account 07-0137.

David N. Lathrop

RESPONSE TO OFFICE ACTION AFTER FINAL REJECTION

Sir:

This communication is submitted in response to the office action mailed November 3, 2004 (referred to herein as "Office Action") and the advisory action mailed March 14, 2005 (referred to herein as "Advisory Action").